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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,562	10/15/2004	Aaron Reel Bouillett	PU020123	4174

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EXAMINER	
NGUYEN, LEON VIET Q	

ART UNIT	PAPER NUMBER
2635	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/511,562	BOUILLETT, AARON REEL	
	Examiner	Art Unit	
	Leon-Viet Q. Nguyen	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/15/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 10/15/2004 was filed after the mailing date of 10/15/2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 10-12, and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogawa et al (US5781463).

Re claim 1, Ogawa discloses an apparatus for determining convergence of an equalizer, comprising:

an equalizer output signal (the output from 1 and 2);

a nearest element decision device (30), the nearest element decision device receiving the equalizer output signal (fig. 8) and creating a decision device output signal containing permissible symbol values (col. 16 lines 45-48, the output of 30); and

a monitoring circuit (6, 31, and 32), the monitoring circuit receiving the decision device output signal (fig. 8, the output of 30) and applying a test criterion to data contained in the decision device output signal so as to determine equalizer convergence (col. 16 line 58-col. 17 line 3, test criterion being a the response to a logic "0" or "1").

Re claim 2, Ogawa discloses an apparatus wherein the equalizer is formed to include an infinite impulse response filter (2).

Re claim 3, Ogawa discloses an apparatus wherein the nearest element decision device is a slicer (30).

Re claim 4, Ogawa discloses an apparatus wherein the monitoring circuit receives the decision device output signal for a predetermined period of time (col. 7 lines 6-11, the selection unit 6 is part of the monitoring circuit) representing an acquisition of a desired number of transmitted symbol values (col. 16 lines 52-54, the logic signal from 30 containing "0" and "1").

Re claim 5, Ogawa discloses an apparatus further comprising a memory (fig. 5), the memory being coupled to the monitoring circuit and being adapted to store decision device output data and test criteria (col. 14 lines 17-20).

Re claim 6, Ogawa discloses an apparatus wherein the test criteria for determining equalizer convergence includes identifying a desired sample of transmitted symbol values (col. 16 lines 58-63).

Re claim 7, Ogawa discloses an apparatus wherein the desired sample of transmitted symbol values includes at least one of every possible symbol value (col. 16 lines 52-54, the logic signal contains the only two possible values "0" and "1").

Re claim 10, Ogawa discloses an apparatus wherein the equalizer output signal includes an image representative datastream containing data packets (col. 4 lines 43-46, the apparatus being a television receiver obtaining a reception image and it is well known in the art that image data can be sent in packets).

Re claim 11, Ogawa discloses an apparatus wherein the monitoring circuit is a microprocessor (31, it is inherently known in the art that a counter is a microprocessor).

Re claim 12, Ogawa discloses an equalizer status monitoring device for use in a digital communication system (fig. 8), the device including an adaptive channel equalizer (1 and 2), a slicer (30) and a monitoring circuit (6, 31, and 32), wherein the digital communications system receives a vestigial sideband modulated signal containing high definition video information (col. 4 lines 43-46, the system being a television receiver obtaining a reception image) represented by a multiple level symbol

constellation (2A-2C), the data having a data frame format constituted by a succession of data frames (it is inherent that a television receiver receive data images in succession), the adaptive channel equalizer generating a first output signal which is input to the slicer (the output from 1 and 2), the slicer generating a second output signal which is input to the monitoring circuit (the output of 30 to 31), the monitoring circuit applying a test criteria to the second output signal to determine convergence of the adaptive channel equalizer (col. 17 lines 4-7, test criterion being a logic "0" or"1").

Re claims 15 and 17, Ogawa discloses a system wherein the test criteria for determining convergence requires identifying at least some transmitted symbol values (col. 16 lines 58-63).

Re claim 16, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 2.

Re claim 18, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 11.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8, 13, 19, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al (US5781463) in view of Nam (US6515713).

Re claim 8, Ogawa teaches an apparatus wherein the monitoring circuit is coupled to the equalizer (the output of 6 to 1 and 2), but fails to teach the monitoring circuit resetting the equalizer when the equalizer diverges. However Nam teaches resetting an equalizer when the equalizer is diverged (col. 2 lines 14-18).

Therefore taking the combined teachings of Ogawa and Nam as whole at the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the method of resetting an equalizer of Nam into the receiver of Ogawa to compensate for channel distortion and perform stable equalization (col. 2 lines 14-18).

Re claim 13, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 8.

Re claim 19, Ogawa teaches in a digital communications receiver including an adaptive equalization filter that desirably achieves a state of convergence (col. 17 lines 4-7, logic state "1" being a high or desirable state) and which undesirably achieves a state of divergence or an invalid state (col. 17 lines 29-32 and lines 41-49, logic state "0"

being a low or undesirable state), a method of monitoring the state of the equalization filter comprising the steps of:

coupling an output signal from the equalization filter to a monitoring circuit (the output of 1 and 2 to 31);

causing the monitoring circuit to examine data contained within the output signal (col. 16 lines 45-48, the input signal containing a logic 0 or 1) for a finite time period (col. 17 lines 16-17, there is some definite input period);

causing the monitoring circuit to apply a test protocol to the examined data (col. 17 lines 4-8 and lines 29-33);

However Ogawa fails to teach where the monitoring circuit resets the equalization filter when the test protocol detects a state of divergence. Nam teaches resetting an equalizer when the equalizer is diverged (col. 2 lines 14-18).

Therefore taking the combined teachings of Ogawa and Nam as whole at the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the method of resetting an equalizer of Nam into the receiver of Ogawa to compensate for channel distortion and perform stable equalization (col. 2 lines 14-18).

Re claim 21, Ogawa teaches a method further comprising the steps of:

coupling the equalization filter output signal to a slicer (1 and 2 coupled to 30);

and coupling the slicer to the monitoring circuit (30 coupled to 31) such that the monitoring circuit examines data generated by the slicer (col. 16 lines 45-48, the input signal containing a logic 0 or 1).

Re claim 22, Ogawa teaches a method wherein the test protocol (col. 17 lines 4-8 and lines 29-33) requires detection of each possible transmitted symbol value within the data generated by the slicer (col. 16 lines 52-57) in order to find that the equalization filter has achieved a state of convergence (col. 16 lines 58-63).

Re claim 23, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 11.

6. Claims 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al (US5781463) in view of Nozue (US4697265).

Re claim 9, Ogawa teaches an apparatus wherein the monitoring circuit is coupled to the equalizer (the output of 6 to 1 and 2), but fails to teach the monitoring circuit resetting the equalizer when the equalizer achieves an invalid state. However Nozue teaches resetting an equalizer if the error rate for some received data becomes too high and exceeds a specific value (col. 1 lines 29-34).

Therefore taking the combined teachings of Ogawa and Nozue as whole at the time the invention was made, it would have been obvious to one of ordinary skill in the

art to combine the method of resetting an equalizer of Nozue into the receiver of Ogawa to prevent divergence of the equalizer (col. 1 line 34).

Re claim 14, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 9.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al (US5781463) in view of Nam (US6515713) and further in view of Nozue (US4697265).

Re claim 20, Ogawa and Nam fail to teach a method further comprising the step of causing the monitoring circuit to reset the equalization filter when the test protocol detects that the equalization filter has achieved an invalid state. However Nozue teaches resetting an equalizer if the error rate for some received data becomes too high and exceeds a specific value (col. 1 lines 29-34).

Therefore taking the combined teachings of Ogawa, Nam and Nozue as whole at the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the method of resetting an equalizer of Nozue into the receiver of Ogawa and Nam to prevent divergence of the equalizer (col. 1 line 34).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on 571-272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/

VU LE
SUPERVISORY PATENT EXAMINER